Over 70-GHz 4.9-V_{ppdiff} InP linear driver for next generation coherent optical communications

Hersent Romain[1,2], *Dupuy Jean-Yves*[1], *Konczykowska Agnieszka*[1], *Jorge Filipe*[1], *Blache Fabrice*[1], *Riet Muriel*[1], *Nodjiadjim Virginie*[1], *Mismer Colin*[1], *Kasbari Abed-Elhak*[2] *and Ouslimani Achour*[2]

[1]*III-V Lab, GIE Nokia Bell Labs-Thalès-CEA Leti*, Palaiseau, France
[2]*Laboratoire Quartz*, ENSEA, Cergy, France

***Abstract*—This paper presents a 86.8-GHz bandwidth 4.9-V_{ppdiff} (peak-to-peak differential) linear electro-optical (E/O) modulator driver fabricated in III-V Lab's 0.7-μm InP DHBT technology. On-wafer measurements exhibit a differential gain of 15.1 dB at 0.2 GHz and a 4.1-dB peaking gain at 51 GHz. Record bandwidth and maximum peaking-frequency, for a lumped linear driver, are obtained. Very high quality 100-Gb/s NRZ and 50-GBd PAM-4 output eye diagrams have been measured. A good measurement and EM-simulation agreement is shown. The InP linear driver power consumption is respectively 0.94 and 1.2 W at 4.1 and 4.9-V_{ppdiff} output swings.**

***Index Terms*—E/O modulator high-speed linear driver, 4-level pulse amplitude modulation (PAM-4). Indium phosphide double heterojunction transistor, over 56-GBd electrical time-domain modulation**

I. Introduction

The unprecedented amount of data exchanged each year and the ever growing number of the internet users generate a global Internet Protocol traffic exponential growth. To keep up with the demand, network operators are heading towards coherent technologies, which, through complex modulation formats (QPSK, n-QAM), allow a net increase in transmitted data rates. Accordingly, electrical time-domain modulation symbol-rate standards are overcoming 56 GBd per channel in PAM-4, as demonstrated in [1] and [2]. Besides, huge amount of transmitted data and multi-channel transceivers means skyrocketing power consumption, a real issue in nowadays' environmental challenges. In this context, [3] has demonstrated an over 80-GHz E/O bandwidth 2.3-V V_π 0.2-dB phase-shifter loss lithium niobate Mach-Zehnder interferometer (MZI). Yet, to ensure a proper optical-carrier extinction ratio ($>$ 20 dB) and thus a high signal integrity, an over 4-V_{ppdiff} output swing linear modulator driver with an over 80-GHz bandwidth is required. Besides, its power consumption must stay under 1 W.

In [4], a linear driver with a 57.5-GHz 4.8-V_{ppdiff} output swing running at 64 GBd in PAM-4 has been demonstrated in BiCMOS SiGe, and in [5] the 37.8-GHz InP HBT linear driver shows a 3-V_{ppdiff} output swing at 28 GBd in PAM-4. Their power consumption are respectively 0.82 and 0.73 W. Both have about 4-dB inductive peaking gain, at respectively 47 and 28 GHz, which aims at performing cable equalization or MZI limited bandwidth compensation. Yet, neither has enough bandwidth to ensure the required signal integrity while operating at over 64-GBd symbol-rates in PAM-4.

In [6] a 5.9-V_{ppdiff} 112-Gb/s distributed differential Selector-Driver which was fabricated in the III-V Lab's technology is reported. However, it was not designed for multi-level modulation formats and is too power-hungry. We thus report a 86.8-GHz 4.9-V_{ppdiff} linear driver implemented in this technology. On-wafer measurements show a differential gain of respectively 15.1 and 19.2 dB at 0.2 and 51 GHz. Large-signal 100-Gb/s NRZ and 50-GBd PAM-4 measurements exhibit high-quality output eye diagrams.

II. Design and architecture

The linear driver was fabricated in the III-V Lab 0.7-μm-width InP DHBT technology, with respectively 380 and 340-GHz f_T and f_{MAX}, a BV_{CE0} of about 4 V, a 65 static current gain and an about 0.9-V $V_{BE_{ON}}$, its fabrication process is described in [7]. 5, 7 and 10-μm emitter lengths are available in this technology. The 1.2x1.5 mm^2 driver die is depicted on figure 1, its circuits' core measures about 0.2x0.6 mm^2, its total power consumption is 0.94 W. The layout drawing was carefully optimized thanks to intense EM-circuit co-simulation. All the passive parts are EM-simulated and then co-simulated using the 0.7-μm InP transistors' electric model.

The linear driver cells have been designed following the impedance-mismatching concept developed in [8]. Figure 2 shows the InP linear driver's schematic view. It is composed of a two-cell linear preamplifier and a linear output-driver. The last one is based on a single following-emitter stage and a cascode differential pair. To obtain an over 4-V_{ppdiff} output swing on a 100-Ω_{diff} load, a biasing current of 40 mA per side is needed. Thus, to relax thermal and reliability constraints, paralleled-transistors on each side have been used. Each transistor is biased at 20 mA, close to f_T peak, hence minimizing the C_{bc} parasitic capacitance. The cascode configuration improves the gain-bandwidth product and highly mitigates the paralleled-transistors-induced input and output impedance matching degradation. As for the bandwidth, the last one is further improved thanks to inductive peaking. Resistive degeneration improves the driver linearity, bandwidth and impedance matching through series-feedback. The

Email : romain.hersent@3-5lab.fr

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preamplifier's first cell is composed of a two-stage following-emitter and a cascode differential pair, it provides a 5-dB differential gain, thus improving the signal-to-noise ratio. Large degeneration resistance were used to improve linearity, input impedance matching and common-mode rejection. The second stage is based on a following-emitter stage and a differential pair. It aims at further decreasing the common-mode gain and improving impedance matching between the input stage and the output driver. To preserve bandwidth, low-ohmic collector resistances are a must at the preamplifier-output driver's interface, due to the summation of transistor's junction capacitances of the output driver stage parallelled-transistors. All preamplifier biasing currents have been decreased to obtain a fair trade-off between its linear-dynamic and power-consumption.

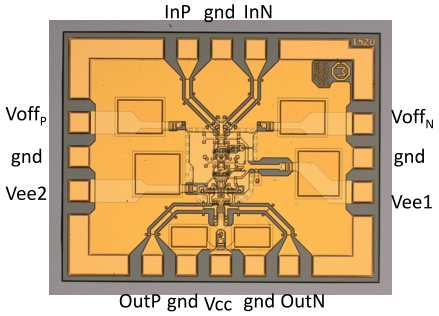

Fig. 1. InP linear driver die

III. Measurement results

4-port and 2-port S parameters were respectively measured using a Keysight PNA N5227A 67-GHz network analyzer from 0.2 to 70 GHz, and up to 110-GHz with a Anritsu ME7808A VNA. Differential S parameters can be retrieved from 2-port measurements, yet, for the differential input/output reflection S parameters, S_{didi}, the input/output crosstalks are required but could not be measured. Figure 3 shows a very good matching between measurement and simulation up to 60 GHz. To save computational resources during simulation, layout simplifications were performed, yet generating a frequency shift above that frequency. Higher accuracy modeling is currently on-going. Measured differantial gain, S_{d2d1}, is 15.1 dB at 0.2 GHz and 19.2 dB at 51 GHz, thus exhibiting a 4.1-dB peaking gain at 51 GHz, which is the highest peaking frequency reported to date for a linear driver. This peaking gain can be used to compensate for the E/O modulator limited bandwidth or for cable equalization. Measured S_{d1d1} and S_{d2d2} are respectively better than -16 dB up to 70 GHz and -10 dB up to 56 GHz, testifying of good impedance matching. The -3-dB bandwidth is 86.8 GHz. To the best of our knowledge it is unprecedented for a linear lumped driver. The low-frequency mismatch between measured and simulated S_{d2d2} may be due to a poor Vcc voltage-source probe decoupling.

Figure 4 depicts the linear driver per-side power transfer function, power-gain and rms-total harmonic distortion (THD), based on the five first harmonics, at 10 GHz, measured on a 50-GHz Agilent E4448A spectrum analyzer, with a differential input. The per-side linear power-gain is about 12.8 dB and the input/output power at 1-dB and 3-dB compression are respectively -3.6/8.0 dBm and 0.34/10 dBm. In the linear region the rms-THD is better than 0.6% and stays under 5% up to an input/output power of -6.2/6.0 dBm. During these measurements, as the peaking gain is uncompensated, e.g no cable equalization, higher harmonics face a higher gain thus degrading the THD.

Large-signal eye diagram measurements have been performed using an Agilent E8257D synthesizer, a SHF 12100B bit pattern generator and an in-house 2 to 1 selector to generate the 100-Gb/s NRZ input signals. An Agilent DCA-X 86100D sampling oscilloscope with 70-GHz remote heads, connected to the output probes through DC-blocks and 20-dB attenuators, not to damage the oscilloscope, were used to observe the output signals. Figure 5 (a) shows the linear driver's single-ended output eye diagram with a 200-mV_{ppdiff} input. A 480-mV_{diff} output eye amplitude and an about 900-mV_{ppdiff} output swing can be observed, resulting in an over 5-dB large-signal peaking gain that can be used for equalization. A clear 4.1-V_{ppdiff} output-swing NRZ eye diagram is depicted on figure 5 (b). The eye amplitude is 3.26-V_{diff} with a 1.66-V_{diff} eye-height, an rms-jitter of 590 ps, a 6.4-ps eye-width and a 6.17 eye S/N. To the best of the authors' knowledge this is the highest quality 4-V_{ppdiff}-class swing 100-Gb/s NRZ eye diagram presented to date at a linear driver's output. The selector output swing was limited to 900-mV_{ppdiff}. Figure 5 (b) right inset shows the measured eye diagram when the driver is replaced by a 1-mm through to serve as a comparison. Poor eye quality is due to a low input level (450 mV_{pp}) together with a 20-dB attenuation of the setup. Using the same setup, yet with an in-house 50-GBd 2-bit DAC, replacing the selector, 50-GBd PAM-4 signals were generated for large-signal multi-level measurement, using some pre-emphasis in scaling DAC's differential output pairs biasing currents. At a 900-mV_{ppdiff} input level the linear driver produces a clear eye diagram with a 3.6-V_{ppdiff} output swing, as depicted on figure 6 (a). Figure 6 (b) shows the linear driver's output eye diagram at a maximum swing of 4.9 V_{ppdiff} with a 1.1-V_{ppdiff} input level. The output stage biasing conditions (Vee2, Vcc) are then modified to prevent further linearity degradations, yet, power consumption is raised to 1.2 W. Corresponding estimated minimum eye amplitude and eye height are respectively 1.3 V_{diff} and 650 mV_{diff}, with a signal total amplitude of 4.1 V_{diff}. To the best of our knowledge, this is one of the highest quality 50-GBd class eye diagram with an over 4-V_{ppdiff} swing at a linear driver's output to date. Horizontal and vertical eye openings are lessened due to uncompensated peaking gain.

IV. State of the art

Table I depicts the state of the art of the linear E/O modulator driver. Although its power consumption is among the highest, the linear driver's bandwidth exceeds 86 GHz, which is unprecedented for a linear lumped driver, ([9], [10] and [11] are distributed amplifiers) as well as a record 51-GHz 4.1-dB peaking gain. PAM-4 50-GBd-class output eye

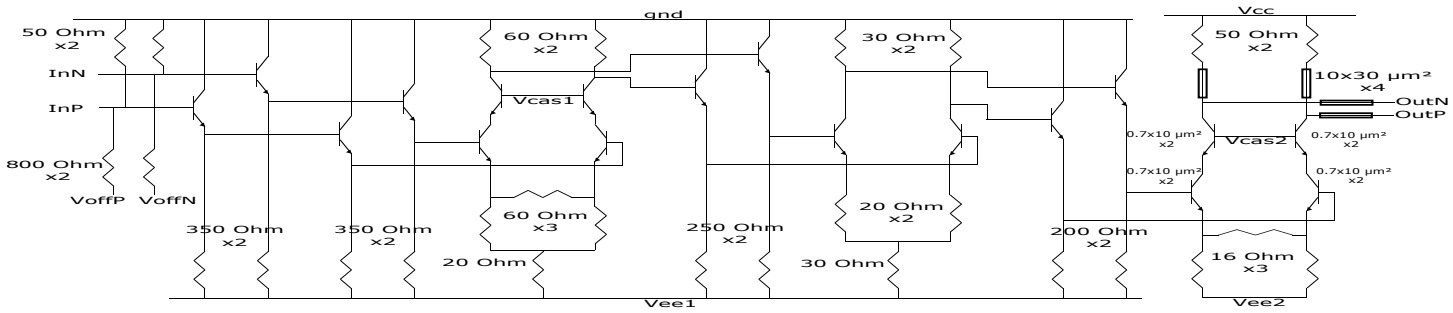

Fig. 2. InP linear driver schematic view

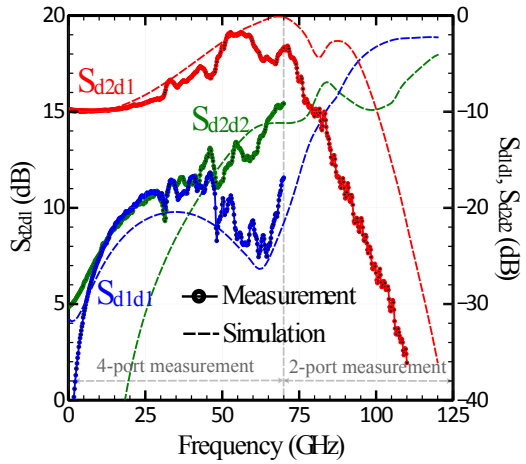

Fig. 3. Measured and EM-simulated InP linear driver S-parameters. Solid lines with symbols depict measurements, broken lines depict simulation results. In red is the differential S parameter gain, S_{d2d1}, in blue and green are respectively the input and output reflection S parameters, S_{d1d1} and S_{d2d2}

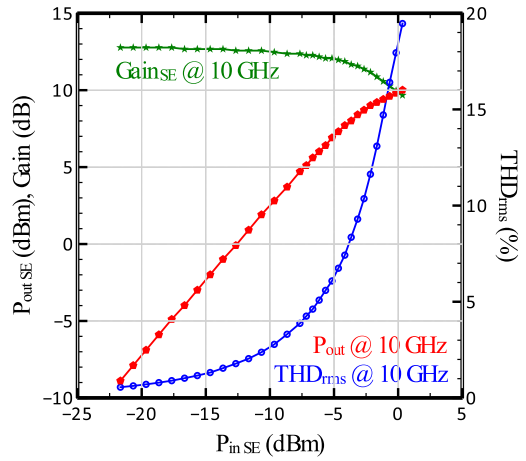

Fig. 4. Measured InP linear driver per-side output-power in red, power-gain in green and fifth-order THD_{rms} in blue at 10 GHz

diagrams are one of the clearest in the state of the art, with [4], with over 4.1-V_{diff} signal total amplitude and over 650-mV_{diff} estimated eye height. Obtained 100-Gb/s-class NRZ eye differential amplitude/height are respectively 1.25/1.43 times greater than in [9] and 1.55/1.38 times those of [10].

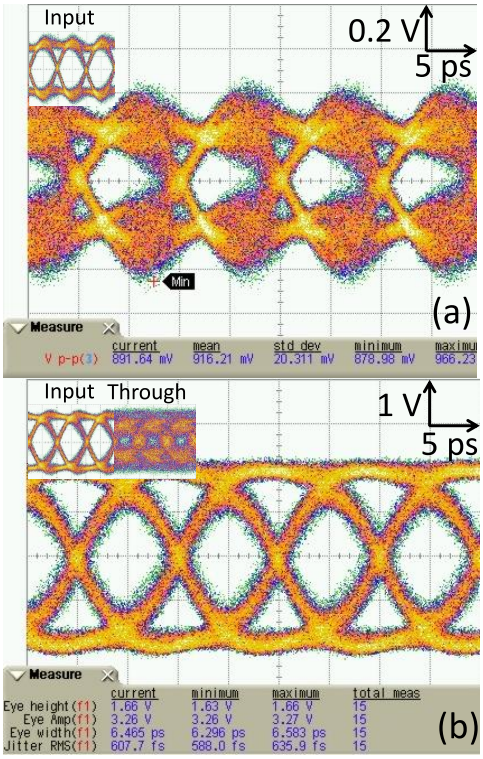

Fig. 5. InP linear driver output eye diagrams: (a) NRZ single-ended output with a 200-mV_{ppdiff} input (inset), (b) NRZ differential output with a 900-mV_{ppdiff} input, insets are respectively the 2:1 selector output eye diagram and the output eye diagram when the driver is replaced by 1-mm through

V. Conclusion

This article presents a 86.8-GHz bandwidth 4.9-V_{ppdiff} swing InP linear driver exhibiting high quality eye diagrams while operating at 50-GBd in PAM-4 or 100-Gb/s in NRZ. It has been fabricated in the III-V Lab's in-house 0.7-μm InP DHBT technology. A record 4.1-dB peaking gain at 51 GHz has been obtained that can be used for equalization. Driver's linear dynamic and power consumption could be improved, notably by reducing preamplifier's number of stages. Thanks to a precise technology-model and intensive EM-circuit co-simulation, most of layout bandwidth-limitations have been overcame, thus resulting in an InP linear driver suitable for next generations Tb/s/channel-class optical communications.

TABLE I
STATE OF THE ART

Parameters	Unit	[5]✦	[12]	[13]✦	[4]✦	[11]✦	[9]✦	[10]	This work
Material	-	InP	SiGe	Si	SiGe	InP	SiGe	SiGe	InP
Technology	-	HBT	BiCMOS	CMOS	BiCMOS	DHBT	BiCMOS	BiCMOS	DHBT
Node	nm	500	250	65	55	250	55	130	700
-3-dB bandwidth	GHz	37.8	-	43	57.5✦	67	>70✦	90	86.8
$\|S_{d2d1}\|$ (<1 GHz)	dB	16.2	14	28	12.8✦	10.7	14✦	12.5	15.1
Maximum peaking gain and frequency✧	dB@GHz	3★@28	4★@19	4★@24❖	4.2@47✦	2.4★@38	-	-	4.1@51
NRZ data-rate	Gb/s	28	-	50	64	100	120/96	120/90	100
NRZ $V_{out_{ppdiff}}$	V	~1.5✦	-	1.45✦	2.3★✦	1.0✦	2.4✦/2.5✦	3/3	4.1
NRZ Differential eye amplitude	V	1.3★✦	-	0.98★✦	2.0★✦	0.6★✦	-/1.3★✦	1.8/2.1	3.26
NRZ Differential eye height	V	1.2★✦	-	0.74★✦	1.7★✦	0.4★✦	-/0.58★✦	0.57★/1.2★	1.66
NRZ Eye S/N	-	-	-	-	-	-	-	-	6.17
NRZ Eye rms Jitter	fs	-	-	-	-	-	429/874	571/609	590
Modulation format	-	PAM-4	PAM-4	PAM-4	PAM-4	PAM-4	PAM-4	PAM-4	PAM-4
Symbol rate	GBd	28	20	40	64/56	56	64/56	45	50
$V_{out_{ppdiff}}$	V	1.5✦	4	2	2.4✦/2.4✦	0.9✦	2.2✦/1.4✦	4	3.6/4.9
Differential total amplitude	V	1.35★✦	-	-	-/2.2★✦	-	-/1.2★✦	3.6	4.1
Differential minimum eye height	V	-	-	-	-/0.62★✦	-	-/0.25★✦	-	>0.65
Power consumption	W	0.73	1.1*	0.18	0.82	0.84	1.1	0.55	0.94/1.2

* *with only 2 bits on over 4.* ✧ *Frequency at maximum peaking gain.* ✦ *Single-ended values. Only single-ended measurements are presented.* ★ *estimated on presented charts.* ❖ *only in minimum gain configuration.*

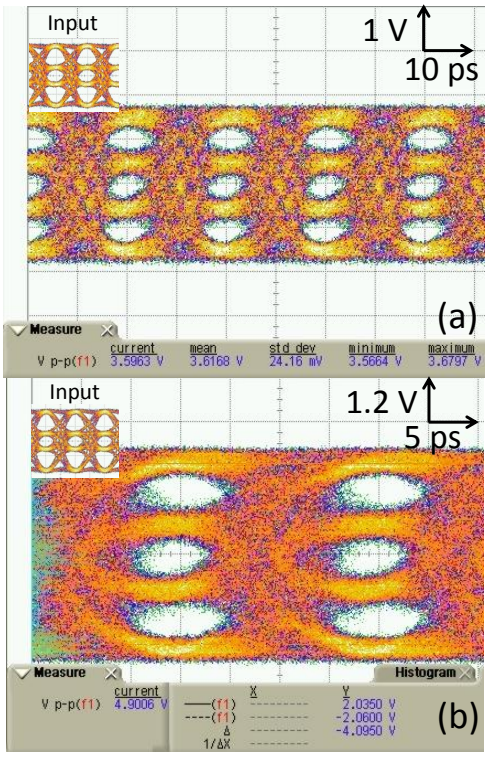

Fig. 6. InP linear driver output eye diagrams: (a) PAM-4 differential output with a 900-mV_{ppdiff} input (inset), (b) PAM-4 differential maximum output-swing with a 1.1-V_{ppdiff} input (inset)

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