InP DHBT Integrated Circuits for High Speed and Low Power Applications

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***Abstract*—Indium Phosphide (InP) Double Hetero-junction Bipolar Transistor (DHBT) technology is characterized by high cut-off frequencies and large breakdown voltages. It is of great interest for the realization of integrated circuits operating at very high speed, with high swing and large analog bandwidth, like modulator drivers for Tb/s optical communications. In this paper, we present an overview of 0.7-µm InP DHBT high speed circuits targeting datacom and telecom fiber-optic applications. We discuss their design and performances, highlighting their power efficiency with respect to other transistor technologies. A 180-Gb/s multiplexing selector, a 64-GBd 3-bit Power DAC and a low power DFF are presented in detail.**

Keywords — HBT, Indium Phosphide, DFF, MUX, DAC, modulator driver, electronic driver, optical communications, PAM format, power efficiency.

I. INTRODUCTION

The development of new services boosts the traffic demand over existing telecom networks. All transmission distances are involved from long-haul inter-continental to datacenter connections. This rapid evolution puts pressure on equipment manufacturers to provide system capable to face the user demand. While 64-Gbaud components and systems are already in development phase, research shifts to higher speed and more complex transmission formats [1, 2].

In this paper we present recent progress in InP DHBT technology and circuits operating at symbol rates higher than 100 GBd and capable of 1-Tb/s transmissions.

We also present another, less explored, aspect of InP circuits, namely their capacity to operate with low power consumption, especially when high speed and high swing are required.

II. TECHNOLOGICAL CONTEXT

The progress in optical and electronic technologies, systems with new transmission formats and advanced DSP algorithms, allow working at higher transmission rates and with increased spectral efficiencies. The standardization of PAM-n modulation format is a particular challenge for the driver-modulator interface. As a result, technological and architectural solutions for 100-GBd operation in PAM-n mode are actively investigated.

While CMOS technologies excel in complex low power digital signal processing, bipolar technologies like SiGe and InP usually provide significantly better performances in several analog and mixed-signal functions, like D/A and A/D data conversion, signal amplification, low noise amplification, especially at high operation speeds.

Traditionally, InP DHBT technology enables the realization of high-speed circuits with high-swing. We will show that it can be also optimized for low power consumption.

Johnson's figure of merit, expressed by $FOM_{Johnson} = f_T \times BV_{CEo}$, where f_T is the gain-bandwidth product of the transistor's current gain and BV_{CEo} its breakdown voltage, shows transistor's capability for combined high-speed and high-swing operation. In Fig. 1, we compare $FOM_{Johnson}$ for different InP HBT technologies in function of emitter width.

It can be noticed that the critical dimension (emitter width) of such HBT technologies is in the range of 0.1 to 1 µm, to be compared to deep sub-micron dimensions necessary for other technologies. This feature releases fabrication constraints and is well adapted for high swing (power) applications.

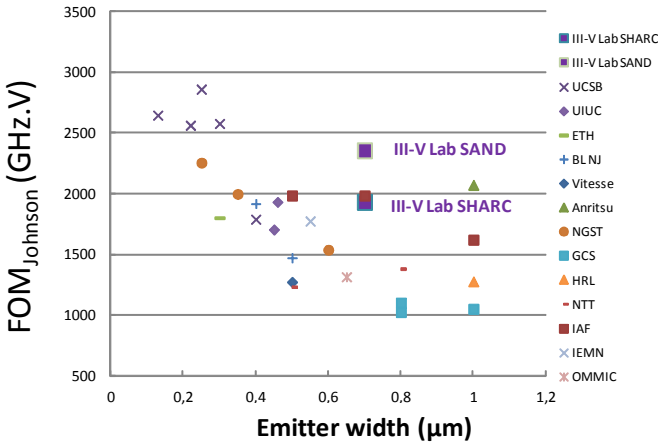


Fig. 1. Johnson's figure of merit for different InP HBT technologies

The integrated circuits discussed in this paper are realized with III-V Lab's 0.7-µm InP DHBT technology [3] exhibiting a 400-GHz f_T and 5-V BV_{CEo} (SHARC process in Fig. 1). The high BV_{CEo} shows clearly the advantage of InP over SiGe bipolar transistors in terms of breakdown voltage.

III. High Speed Electronic Circuits for Optical Transceiver

In [4], Raybon *et al* demonstrated how the particular properties of circuits realized in InP DHBT technology can pave the way to very high speed optical transceivers. Below, we present, as an example, two electrical devices (multiplexing selector and Power DAC modulator driver) designed and fabricated in InP DHBT technology. Some key optical systems experiments enabled by these components are also shown.

A. Multiplexing selector

N:1 Electrical Time Domain Multiplexing consists in combining N input signals into one output stream by reducing by N the time slot attributed to each input data. This technique is used in transmission systems to increase the channel transmission capacity. Very high speed Multiplexers (operating over 100 Gb/s bitrate) are necessary for optical communication experiments, where maximal transmission capacity is sought.

In [5], a 165-Gb/s 4:1 multiplexer fabricated in InP DHBT technology was presented. Recently, we have realized a 2:1 multiplexing selector measured at 180 Gb/s, enabling experiments up to 204 Gb/s.

To obtain operation at such high speed, special effort needs to be deployed during design, measurements and packaging. As we aim at 200-Gb/s operation, even the input parts (data and clock buffers) working at half-rate, need to be carefully designed to support respectively 100-Gb/s speed and 100-GHz frequency. The Gilbert cell architecture is chosen for selector core. Passive peaking is applied to increase bandwidth of different blocks.

The circuit is composed of 48 transistors and its power consumption is 0.5 to 0.8 W for a differential output amplitude of 250 to 730 mV. The chip footprint is 1.2 x 1.5 mm².

In Fig. 2, the output eye diagram of the selector at 180 Gb/s is presented. The clock phase margin is measured to 3 ps. The selector's output signal has 2x200 mV amplitude and 450-fs rms (root mean square) timing jitter. The input 90-GHz clock rms timing jitter is 270 fs.

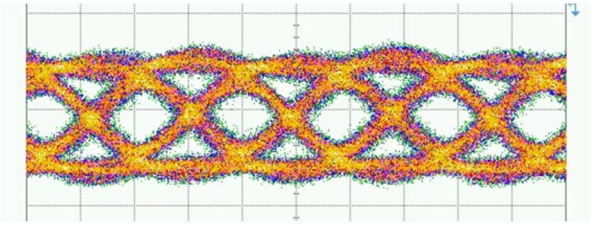


Fig. 2. InP DHBT 2:1-selector single-ended electrical output signal measured on wafer at 180 Gb/s (vertical scale: 100mV/div, horizontal scale: 3ps/div.).

B. Power DAC modulator driver

In optical transmitter, the modulator driver is placed at the end of the electrical part and is directly connected to Electro-Optical (E/O) modulator. Specifications for this circuit are particularly demanding, as it should operate at the highest speed (symbol rate) compared to successive electronic stages and generate swing necessary to optimally drive the modulator.

The Power-DAC architecture was first proposed by III-V Lab in 2011 [6], followed by multiple new implementations allowing the realization of record optical experiments (see references in [7]).

The Power-DAC operation principle consists in simultaneous realization of two operations: (i) weighted summation of *n* input data streams to create multilevel signals and (ii) amplification, necessary for a modulator driver. Additionally, all circuit elements are operating in digital (saturated) mode instead of analog mode.

The last version, a 3-bit Power-DAC integrated with three multiplexing selectors is named SPDAC. This architecture facilitates RF inputs interfacing and packaging as it requires half-rate input signals. In Fig. 3, we show the circuit microphotograph and typical output signal eye-diagram measurements.

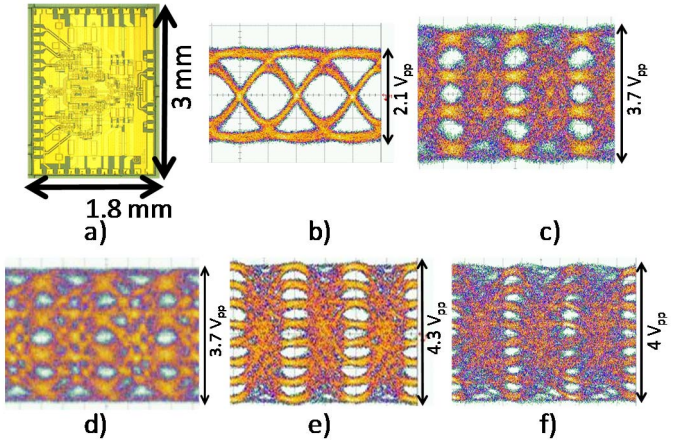


Fig. 3. InP DHBT SPDAC circuit microphotograph (a) and measurements: b) PAM-2 at 100 GBd (100 Gb/s), c) PAM-4 at 88 GBd (176 Gb/s), d) PAM-4 at 100 GBd (200 Gb/s), e) PAM-8 at 50 GBd (150 Gb/s), f) PAM-8 at 64 GBd (192 Gb/s).

The chosen SPDAC architecture has proven to be very practical. The operation in different modes (1/2/3-bit) can be obtained with simple modification of dc controls. The integration of the driver with an array of multiplexing blocks enables the interface with electronics at half-rate and makes a significant difference when operating at extreme speeds.

C. Extreme speed and capacity optical experiments

To satisfy the constantly growing transmission traffic, various methods are intensively investigated. Different aggregation techniques (WDM, SDM) are explored, while the transmission capacity per single wavelength is rapidly progressing. Multilevel formats (PAM-n and m-QAM) are of particular interests as they provide high spectral efficiency. However On-Off Keying (OOK) formats have important advantages in implementation simplicity and capacity for long-distance transmission. Both circuits presented in this section enabled various state-of-the-art transmission experiments in data-center and long-haul domains.

Two experiments using the new multiplexing selector were presented as post-deadline papers at OFC'18. In [8], 204-GBd

OOK intensity modulation and direct detection (IM-DD) transmission for data-center communication was demonstrated on 20 km distance. In [9], 180-GBd (720 Gb/s) all-ETDM single-carrier polarization-multiplexed QPSK with coherent detection was investigated. Transmission over 4480 km was demonstrated.

In [10], the first all-ETDM single-carrier and single-modulator 1.08-Tb/s (90-GBd PDM-64-QAM) transmitter is demonstrated using SPDAC modules. Six single-ended 45-Gb/s signals are 2:1-multiplexed and amplified into a differential 90-GBd PAM-8 4-V_{pp} differential output signal, driving an I/Q modulator. At the receiver side, a high speed coherent intradyne receiver is connected to a 4-channel 160-GS/s real-time oscilloscope for off-line DSP. In [11], a single-carrier, single-polarization, intensity modulation and direct-detection transceiver for intra-datacenter networks is reported. Half-rate (42 and 50-Gb/s) input signals are multiplexed and coded to produce 84-GBd and 100-GBd PAM-4 outputs. C-band transmission over 1 km and 500 m is demonstrated.

IV. Low power circuits in InP DHBT technology

CMOS technologies are well adapted to realize complex low power digital processing circuits. We will show that for circuits operating at high speed and/or high-swing, InP DHBT technology can not only fulfill high performance specifications, but can demonstrate low power operation with higher power efficiency in the region where direct comparisons are possible.

As an example, let us consider the design of ultra-low power transceiver front-end for 94-GHz phased arrays presented in [12]. In this design, a 130-nm InP DHBT technology was used with transistors achieving f_T/f_{max} of 520/1100 GHz respectively. The transceiver demonstrated significantly lower power consumption compared to SiGe BiCMOS realizations.

In this section, we present some guidelines for low power design and discuss two use cases: low power D-type Flip-Flop (DFF) and SPDAC circuit operating as PAM-8 driver.

A. Low power and high power efficiency design for InP DHBT technology

In Fig. 4 the frequency characteristics of recent InP DHBT transistors from III-V Lab are shown.

Two regions of operation are identified. For low power operation and with limited bitrate/frequency design, transistors are operating in **LP region** and less consuming architectures can be chosen. For circuits operating in 50-GBd rate we chose f_T/f_{max} zone below 100-150 GHz, and Current Mode Logic (CML) architecture, rather than the Emitter Coupled Logic (ECL) consuming more but providing higher operation frequency. For circuits with the highest frequency performances, transistors work in **HF zone**.

B. Low power DFF

The DFF is a key building block present in most digital circuits, like (de-)multiplexing circuits. DFF and static divider having similar structures are often used as a technology benchmarks to evaluate the maximal operation speed.

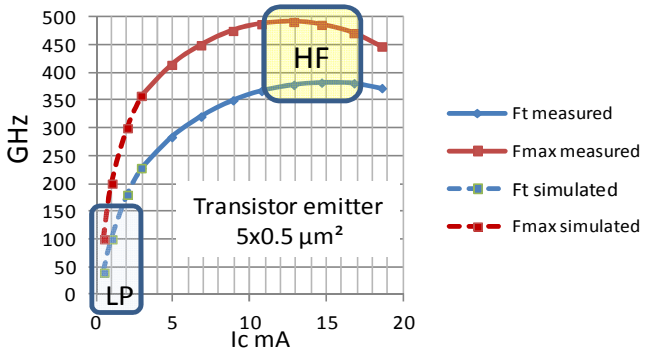
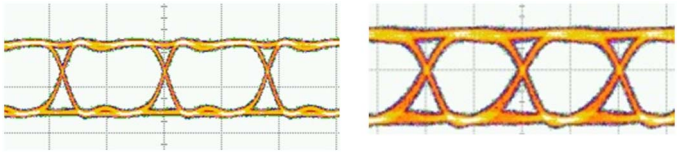


Fig. 4. f_T and f_{max} (GHz) of 5x0.5-µm² (emitter area) transistor in function of collector current (I_C, mA). Low Power (LP) and High Frequency (HF) operation regions are identified.

We realized a family of DFFs using different architectures. Specifically Master-Slave DFFs were designed using CML and ECL architectures. CML-DFF were measured at 28 Gb/s and showed very good quality output eye with 5-6-ps rise/fall time, rms timing jitter of 0.3 ps and S/N ratio = 15. The Clock Phase Margin (CPM) was 22 ps (with bit period equal to 35 ps). With 300-mV differential output swing this circuit consumes 40 mW. The ECL-DFF operating at 50 Gb/s with 400-mV output consumes 200 mW. In Fig. 5, we show the output signals of both DFFs.



(a) (b)

Fig. 5. Single-ended output signal of InP DHBT low power DFFs: 40-mW 300-mV CML-DFF at 28 Gb/s (a); 200-mW 400-mV ECL-DFF at 50 Gb/s (b).

In [13], the comparison of power consumption for DFFs operating in the speed range 30-90 Gb/s was presented.

In Fig. 6, the comparison of DFFs realized with different semiconductor technologies in 25-50 Gb/s range is presented. It can be seen that the power efficiency of InP DHBT DFFs reported is very competitive, compared to traditionally low power silicon counterparts.

C. Power DAC power efficiency

In [14], a 56-Gb/s PAM-4 VCSEL transmitter is presented, using an InP DHBT driver able to operate in PAM-2/4/8, yielding a 2-pJ/bit energy efficiency in PAM-4 at 50 GBd, making it one of the most energy efficient driver for operation above 40 Gb/s.

The output buffer of SPDAC is composed of 3 preamplifiers with adjustable gain and amplifying cascode combiner delivering a differential signal. The block diagram of the output buffer is presented in Fig. 7.

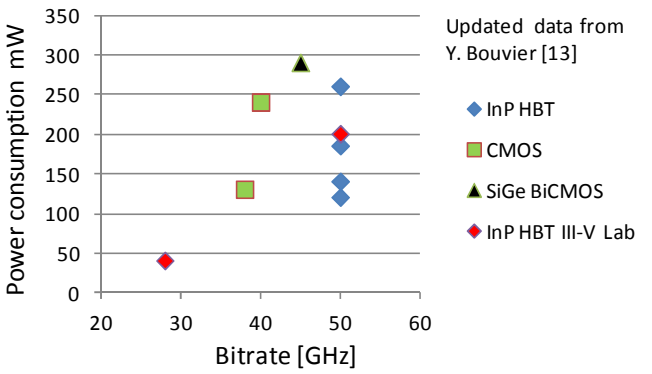


Fig. 6. Comparison of DFF performances.

The driving output buffer is composed of 39 transistors and its power consumption is 1 W when the PAM-8 output swing is 4.3-V_{pp}.

3-bit Power-DACs, presented in section III.B, were driving modulators in 1-Tb/s transmitter based on Dual-Polarisation 90-GBd 64-QAM format demonstrating 1080 Gb/s transmission capacity. In this experiment, mentioned in III.C, each SPDAC was operating in PAM-8 format at 90 GBd (electrical speed of 270 Gb/s) with 4.3-V_{pp} output swing. This result demonstrates excellent power efficiency of this driver equal to 0.88 pJ/(b·V).

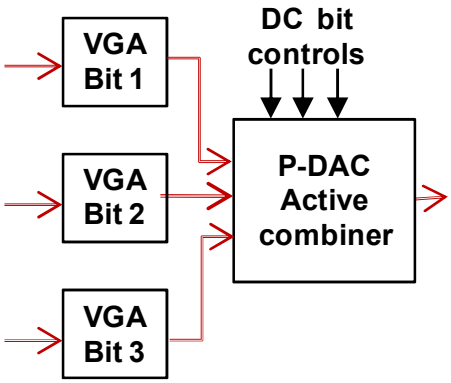


Fig. 7. SPDAC's driving output buffer's architecture with three Variable Gain Amplifiers (VGA).

V. Conclusions

Operating at high speed and low power requires advanced transistor technology and circuit design methodology. We have demonstrated that the InP DHBT technology is particularly well suited in that respect. In particular, reaching 400-GHz f_T/f_{max} and 5-V breakdown voltage, III-V Lab's 0.7-µm InP DHBT technology has enabled the demonstration of a record 180-Gb/s 2:1-mutiplexing selector, a large swing 3-bit Power-DAC with 2:1-multiplexing inputs with a maximum sample rate of 100 GS/s, as well as low power DFFs. These circuits have enabled several pioneering optical transmission experiments pushing further the frontier of symbol rate beyond 100 GBd for ever higher capacities per optical carrier without compromising for architecture complexity. These realizations are believed to be key technological enablers and accelerators to help terabit transport and connectivity come to reality in a close future.

Acknowledgement

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