InP DHBT D-Band Stacked Power Amplifier

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***Abstract*—In this paper, a D-band stacked power amplifier in a 0.7-µm InP DHBT technology is reported. The power amplifier is implemented using a novel finite-ground elevated coplanar waveguide (FG-ECPW) interconnect environment leading to low-loss power combination. A miniaturized Wilkinson power combiner demonstrates a low loss of ~0.5 dB when measured in a back-to-back configuration. A fabricated two-stage two-way combined triple stacked power amplifier demonstrates a small-signal gain of 14.9 dB at 118 GHz and a -3 dB bandwidth from 111.2 GHz to 130.6 GHz. The amplifier reaches a peak output power of 17 dBm at 120 GHz. The corresponding large-signal power gain is 9 dB and the PAE is 7.2%**

Keywords—D-band, power amplifiers, indium phosphide, double heterojunction bipolar transistor (DHBT), stacking.

I. Introduction

Global interconnectability or the so-called Internet of Everything (IoE) is foreseen within the 6G paradigm. The millimeter-wave frequency range above 100 GHz is attractive for 6G wireless networks due to the increased available spectrum and possibility for compact MIMO based systems [1]. The D-band frequency range from 110 – 170 GHz has been identified as suitable for 6G high-capacity mobile communications.

The power amplifier remains one of the most critical components for wireless networks operating above 100 GHz. This is due to the increased power loss of the passives and physical limitations of the used transistor technologies. Among the various semiconductor technologies, InP HBT technology has proven superior for power amplifiers above 100 GHz [2]. Recently, several authors have reported InP HBT based D-band power amplifiers with high output power and good efficiency [3]-[6]. Most of these works [3]-[5] have been fabricated in the 250 nm InP HBT technology from Teledyne featuring f_T and f_{MAX} of 350-GHz and 600 GHz, respectively, with a breakdown voltage of 4.5 V. In [6], a 130 nm InP HBT technology from Teledyne with f_T/f_{MAX} of 521 GHz/1.15 THz and breakdown voltage of 3.5 V has been employed.

Here we report on a D-band power amplifier in III-V Lab's InP HBT technology. The technology used has a relaxed 0.7-µm node and transistors with up to 400 GHz f_T/f_{MAX} and >4.5 V breakdown voltage. To achieve sufficient power gain in the D-band a triple stacked unit power cell is proposed. The power amplifier employs a novel low-loss finite-ground elevated CPW interconnect environment. To achieve a good balance between gain and output power a two-way combined stacked power stage is combined with a stacked driver stage.

II. Technology

A. InP DHBT Technology at III-V Lab

The InP DHBT structure was grown on a 3-inch semi-insulated InP substrate by *IntelliEPI*. The transistor technology is the same as the one described in [7]. InP DHBT devices with an emitter width of 0.7 µm and emitter lengths varying from 5 to 10 µm are available for design. The 0.7 × 5 µm^2 device has maximum f_T and f_{MAX} of 340 GHz and 420 GHz, respectively, at a collector current density of J_c~6 mA/µm^2 and V_{ce}=1.6 V. The breakdown voltage is larger than 4.5 V and the static current gain β is around 40. Despite the relaxed emitter node the devices from III-V Lab show a favorable power dissipation – speed product thus emphasizing the technology's ability to switch high power at its maximum speed. Several record breaking implementations of high-speed drivers, analog multiplexer (AMUX) and power-digital-to-analog converters (DACs) have been achieved using this technology [8]-[10].

For millimeter-wave power amplification a two-finger InP DHBT with individual emitter length of 10 µm has been chosen to maximize the output power per device while still allowing for a sufficient power gain at D-band frequencies. The InP DHBT single-finger devices have been modeled using a modified UCSD HBT large-signal modeling approach (for details see [11]). This modeling approach allows the individual devices to be combined into multi-finger structures taking the electromagnetic and thermal interaction between fingers into account.

B. Finite-Ground Elevated CPW Interconnects

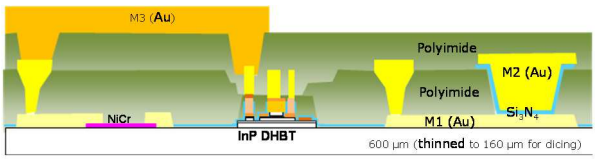

Fig 1. Schematic cross section of the InP DHBT technology.

For circuit design the technology has three Au-based interconnect layers separated by thin (~1.8 µm) polyimide dielectrics. The technology also provides Si_3N_4 MIM capacitors and NiCr thin-film resistors with 40 Ω/sq. A schematic cross section of the technology is shown in Fig. 1. The rather low separation between the metal layers means that thin-film microstrip lines are not an option for low-loss interconnects. Instead CPW based interconnects must be used. As the frequency of operation increases the risk of multi-modal propagation also increases. This is especially the case for CPWs with a backside metallization either due to a

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chuck in an on-wafer characterization environment or due to a metallic carrier in a package. As the technology does not allow through substrate vias, it is advisable to employ so-called FG-CPW interconnect structures [12]. The availability of the three metal layers allows an elevated CPW structure to be exploited. In the elevated CPW structure the top metal (M3 in Fig.1) is used as the signal conductor while the second metal (M2 in Fig.1) is used to form the ground plane. The elevated CPW (ECPW) structure can implement high-impedance transmission lines with lower loss compared to a normal CPW structure [13]. The lowest metal layers (M1 or M2 in Fig.1) can be used to implement underpasses required to connect the ground planes together at CPW discontinuities. The capacitive loading coming from these underpasses must be compensated in order to reduce reflection losses.

To demonstrate the low-loss potential of the proposed FG-ECPW interconnect environment a miniaturized Wilkinson power combiner is designed. The capacitive loading from the underpasses is exploited in the design to form reduced size quarter-wave transformers according to the design approach in [14].

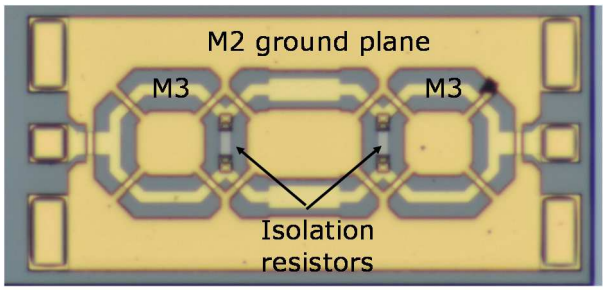

Fig.2. Micrograph of miniaturized Wilkinson power combiner in a back-to-back configuration.

Fig. 2 shows a micrograph of the miniaturized Wilkinson power combiner in a back-to-back configuration for easy testing. The size of the miniaturized Wilkinson power combiner is 317 ×354 μm^2 without pads but including the ground plane. The measured results in the D-band are shown in Fig. 3 and compared to 3D electromagnetic (EM) simulations using HFSS. A low-loss characteristic is observed over the whole D-band frequency range. The insertion loss is ~1 dB at 140 GHz which result in a loss of only ~0.5 dB for the individual Wilkinson power combiner. Over the whole D-band the insertion loss varies from

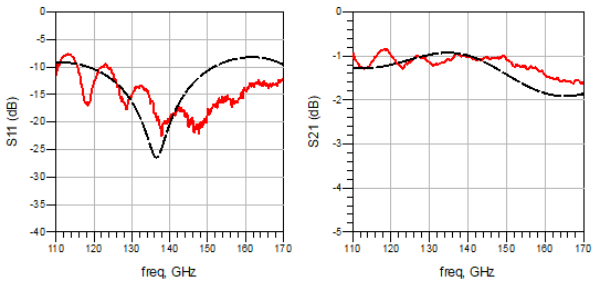

Fig. 3. Measured S_{11} (left) and S_{21} (right) for miniaturized Wilkinson power combiner in a back-to-back configuration. The dashed lines are HFSS simulations.

approximately 0.8 dB to 1.8 dB verifying the low-loss potential of the FG-ECPW interconnect environment.

A library of compensated FG-ECPW structures such as Tee-junctions, bends and crosses has been created based on calibrated EM simulations in Keysight's ADS Momentum and are available for circuit design. The transition from the RF pads to the FG-ECPW interconnects has been modeled in HFSS.

III. Circuit Design

A. Triple Stacked Power Cell Design

The individual power cells are designed using the stacked

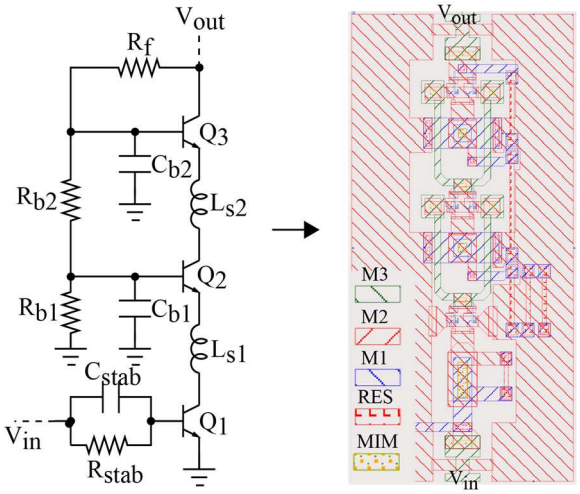

Fig. 4. Schematic and layout of stabilized triple-stacked power cell.

device concept [1]. Stacking allows the limited breakdown voltage for each individual device to be overcome by proper alignment of their respective collector voltage waveforms. Due to layout parasitic effects, however, this alignment of the collector voltage waveforms becomes progressively difficult to achieve as the number of stacked devices increases. Therefore, as shown in Fig. 4, the number of stacked devices is limited to three for the power cell to be used at D-band. For maximum gain the individual transistors in the stack is biased in class-A. The triple-stacked power cell is stabilized by a parallel input RC network (R_{stab}, C_{stab}) and by a resistive feedback network consisting of R_f, R_{b1} and R_{b2}. The resistive feedback network also provides the base bias voltage for the upper devices in the stack. The triple stacked power cell is optimized using an EM-circuit co-simulation approach in Keysight ADS. For the EM simulation using Momentum the active devices in the layout are substituted with internal ports referenced to the global ground plane. The optimized triple stacked power cell shows a linear power gain of 8 dB at 140 GHz. The large-signal simulations shows P_{1dB} of 11.8 dBm, P_{sat} larger than 14.2 dBm, and peak PAE of 6.5%.

B. Two-Stage Two-Way Combined Power Amplifier

The schematic representation of the two-stage two-way combined power amplifier is shown in Fig. 5. The driver stage consists of a single triple-stacked power cell. In the power stage two triple-stacked power cells are combined using a miniaturized Wilkinson power combiner. To adapt the outputs of the individual power cells to the input of the Wilkinson power combiner a single stub matching network is employed. For compactness, the open-circuited stubs are implemented using thin-film microstrip lines between the top

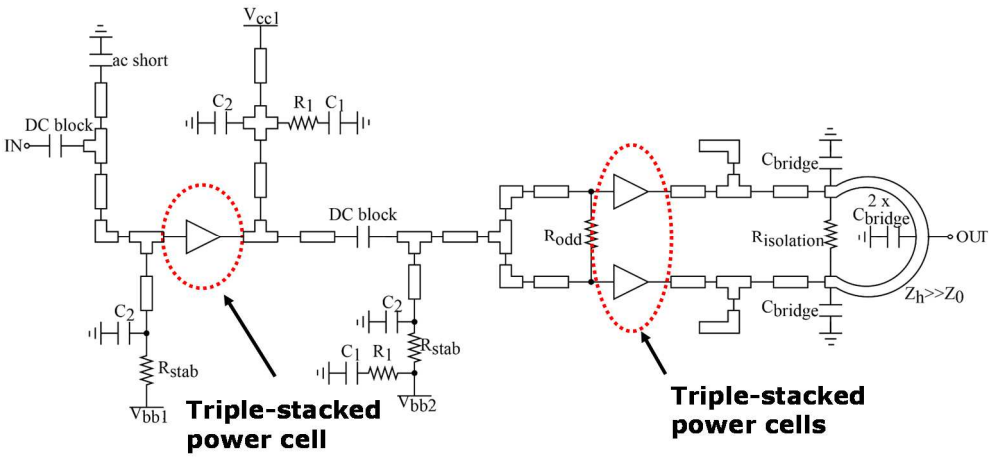

Fig. 5. Schematic representation of two-stage two-way combined power amplifier.

metal (M3) and the ground plane (M2). An inter-stage matching network with tee-junction two-way power splitting matches the power cell in the driver stage to the power cells in the power stage. For out-of-band stabilization, resistors are placed into the bias networks and an odd-mode stabilization resistor is placed between the inputs of the two power cells of the power stage.

A micrograph of the fabricated D-band power amplifier MMIC is shown in Fig. 6. The FG-ECPW interconnect environment is clearly visual. The chip size is 2.4 × 1.5 mm^2.

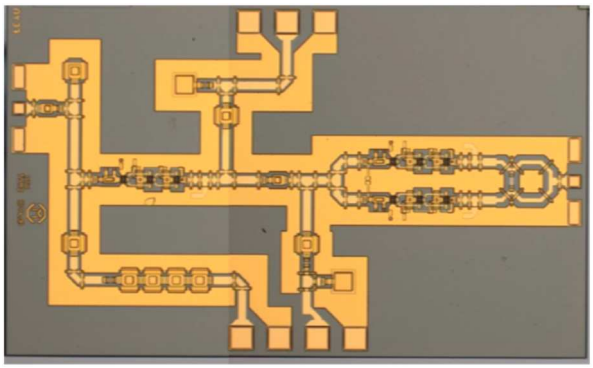

Fig. 6. Chip micrograph of the D-band power amplifier. The chip size is 2.4 × 1.5 mm^2.

IV. Experimental Results

The fabricated D-band power amplifier was measured on-wafer using 125 µm pitch WR-6.5 ground-signal-ground probe tips from GGB Industries. The biasing was provided through DC probes de-coupled at the probe tips.

A. Small-Signal Characterization

For the small-signal characterization an Anritsu 37397D lightning vector network analyzer (40 MHz – 65 GHz) with WR-6.5 D-band frequency extenders from VDI were used. In the S-parameter measurements the power stage is biased at a supply voltage of 6.4 V and supply current of 61.8 mA. The driver stage is supplied from 6.0 V and draws a current of 20.1 mA. The measured and simulated forward S-parameters (S_{11} and S_{21}) are shown in Fig. 7. The amplifier demonstrates a measured small-signal gain of 14.9 dB at 118 GHz. The measured -3 dB bandwidth is from 111.2 GHz to 130.6 GHz. A shift in the matching to lower frequencies is

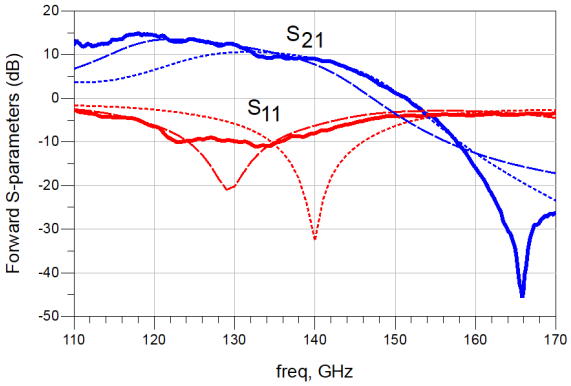

Fig. 7. Measured (solid lines), nominally (dotted lines) and retro (dashed lines) simulated forward S-parameters.

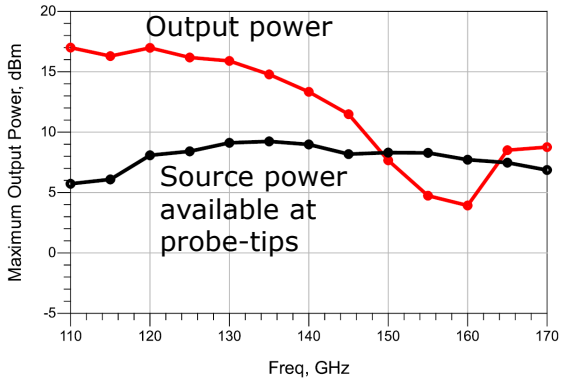

Fig. 8. Measured large-signal frequency response.

observed in the measurements as compared to simulations. As a result the measured gain peak is also shifted down in frequency. Retro simulations using an updated transistor model based on measurements of InP DHBTs on the same wafer as the power amplifier, additional bridge capacitance of 4 fF, and 30 fF increase in the base capacitances of the stack can reasonable well explain the shift in matching to lower frequencies.

B. Large-Signal Characterization

The large signal characterization was performed using a medium power broadband source consisting of a RPG AFM12 × 12 multiplicator (110 – 170 GHz, typ >+10 dBm) followed by a WR-6.5 waveguide attenuator. The output

power was measured using an Ericksson PM5 power meter with WR-6.5 to WR-10 adaptor. At first, the power out of the broadband source is measured at the waveguide interface before the probe. Next the output power is measured using an on-wafer thru. Neglecting the losses of the on-wafer thru and assuming the input and output probes to be identical allows the measured powers to be referenced to the probe tips.

In the large-signal measurements the supply current is increased to 32.6 mA and 65.0 mA for the driver and power stage, respectively, while the supply voltages from the small-signal characterization are kept. Fig. 8 shows the measured output power versus frequency at maximum available source power (included in Fig.8 for reference). The maximum output power of +17 dBm is measured at 120 GHz. This corresponds to a large-signal power gain of 9 dB and a PAE of 7.2%. The output power remains above +16 dBm in the frequency range from 110 – 130 GHz.

V. Conclusion

A two-stage two-way combined stacked power amplifier for D-band wireless communications has been reported. The power amplifier is implemented using a FG-ECPW interconnect environment leading to low-loss impedance matching and power combination.

Acknowledgment

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