Extreme Speed Power-DAC: Leveraging InP DHBT for Ultimate Capacity Single-Carrier Optical Transmissions
(invited)

Agnieszka Konczykowska
Jean-Yves Dupuy, Filipe Jorge, Muriel Riet, Virginie Nodjiadjim

III-V Lab, joint laboratory of Nokia Bell Labs, Thales Research and Technology and CEA/LETI, 1 Av. A. Fresnel, 91767 Palaiseau, FR
agnieszka.konczykowska@3-5lab.fr

Abstract: With 100-GBd operation and 4-V_{pp_diff} swing, InP DHBT Power-DAC enabled experiments with different types of E/O modulators. Single-carrier 100-GBd PAM-4 IM/DD transceiver for datacenters and 1.08 Tb/s transmitter (90-GBd PDM-64QAM) were demonstrated.
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1. Introduction

In the last decades, an unprecedented demand for greater optical transmission capacities has been observed in a wide range of domains from short-reach to long-haul systems. This increasing demand is mirrored by the intensive industrial activity to satisfy the exponential growth of the IP traffic. Research activities are engaged to explore various alternatives to increase throughput of optical systems taking into account additional criteria like spectral efficiency, reach, complexity, power consumption and cost. The progress in optical and electronic technologies, systems with new transmission formats and advanced DSP algorithms, allowed working at higher transmission rates and with increased spectral efficiency. In this context, multilevel coded transmission and m-ary Quadrature Amplitude Modulation (m-QAM) are of particular interest.

The need for high-speed optical interfaces is driving research towards higher-and-higher all-electronically-generated symbol rates, in order to minimize the number of parallel opto-electronic transmitters and receivers.

Very high speed electronic digital-to-analog converters (DACs) for optical communication transmitters were realized in different semiconductor processes. In [1], an 8-bit 100-GS/s CMOS DAC is presented, able to generate electrical output signals in PAM-4 at 50 GBd and PAM-8 at 40 GBd, with ≈300-mV_{pp} amplitude. In [2], a 60-GS/s 6-bit DAC is reported, showing PAM-4 electrical signal at 64 GBd and PAM-8 signal at 60 GBd with limited eye openings and 2.8-V_{pp_diff} maximal differential amplitude. A transmission experiment implementing PDM-64-QAM at 72 GBd (864 Gb/s) was demonstrated with a 6-bit DAC realized in SiGe process [3]. Circuits and experiments using InP processes will be discussed in section 2.

In this paper, we start by presenting in section 2 the technological context and InP HBT realizations. Section 3 is devoted to the presentation of Power-DAC (PDAC) architectures and main circuit results. In section 4, we present different optical system experiments using PDAC and Selector-PDAC (SPDAC) modules. We conclude with perspective section.

2. Technological context and InP HBT high-speed ICs

In Fig. 1, the Johnson's figure of merit, plotting breakdown voltage (BV_{CEo}) in function of transition frequency (f_T) for Si-, InP- and GaN-based semiconductor processes is shown. BV_{CEo} and f_T performances illustrate the suitability of different materials for the realization of high speed and high voltage transistors.

Today's speed challenge for electronic driver interface is 100-GBd operation in PAM-N mode. As shown in Fig.1, transistors with 300-400-GHz f_T and 4-6-V BV_{CEo}, as required to realize 100-GBd modulator drivers, can be implemented in InP DHBT technology. The critical dimension (emitter width) of such III-V processes is in the range of 0.1 to 1 μm, to be compared to deep sub-micron dimensions necessary for other technological processes. This feature releases fabrication constraints and is well adapted for high swing (power) applications.

Array transceivers on polymer platform using InP HBT drivers and TIAs, for serial 100-Gb/s operation, targeting intra-data center networks, have been reported in [4]. In [5], a 6-bit InP HBT DAC integrated with MUX stages has been realized. This circuit has been used in an optical experiment demonstrating 75-GBd PDM-16QAM WDM transmission with 1-Tb/s capacity over two carriers [5].

The InP HBT technology also enables the design of high-speed circuits with optimized low power consumption. In [6], a 56-Gb/s PAM-4 VCSEL transmitter is presented, using an InP HBT driver able to operate in PAM-2/4/8,

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yielding a 2-pJ/bit energy efficiency in PAM-4 at 50 GBd, making it the most energy efficient driver for operation above 40 Gb/s.

In the next section, we present PDAC drivers realized in III-V Lab's internal 0.7-µm InP DHBT process [7], with f_T/f_{MAX} and BV_{CEo} equal to 400/370 GHz and 5 V, respectively. The $(f_T.f_{MAX})^{0.5} \cdot BV_{CEo}$ figure of merit combining frequency and swing potential is around 2000 GHz · V.

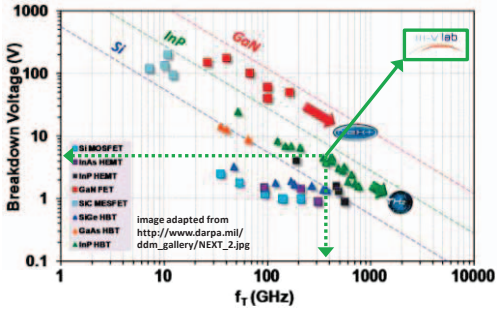


Fig. 1. Johnson's figure of merit: breakdown voltage (BV_{CEo}) vs. transition frequency (f_T)

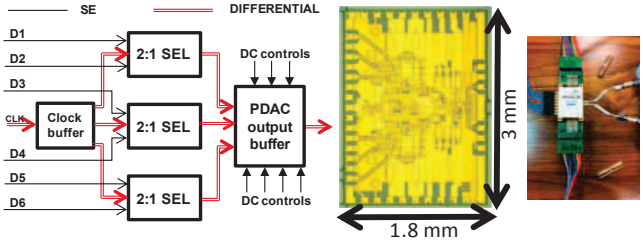
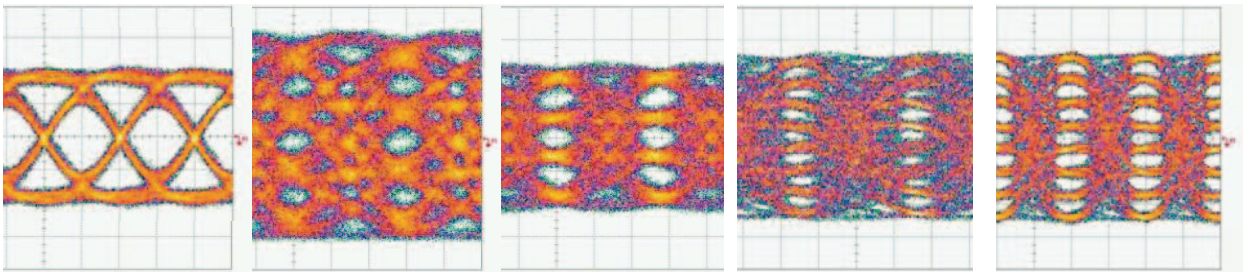


Fig. 2 SPDAC: block diagram, chip and module photographs

3. Power-DAC architectures, module and performances

The Power-DAC concept was first proposed in 2010, when m-ary PAM and QAM modulation formats started to be intensively investigated. Contrary to the mostly used transmitter architecture, with DAC component followed by broadband linear amplifier, the Power-DAC principle consists in simultaneous realization of two operations: (i) combination of n input data streams to create multilevel signals and (ii) amplification, necessary for a modulator driver. Additionally, all circuit elements are operating in digital instead of mixed digital-analog mode. 3-bit power-DAC has been realized, but this concept can be applied to an arbitrary number of bits. PDAC is in general composed of two main integrated blocks: (i) the input interface operating on binary signals and (ii) active combiner/amplifier. Various versions of Power-DAC IC have been realized over the years: P-DAC driving buffer only, P-DAC integrated with an array of DFFs for retiming and reshaping [8] and SPDAC [9] where the driving buffer is integrated with multiplexing stages (selectors).

SPDAC architecture, microphotograph of the IC and module are presented in Fig. 2. SPDAC circuit can operate at high symbol rate in PAM-2, PAM-4 and PAM-8 formats when coding 1, 2 or 3 bits of information in a single symbol period. The driving buffer based on PDAC concept provides signal with high amplitude (> $4V_{pp}$ for PAM-8) with no need for further linear amplification. Specific controls implemented in the output buffer allow to pre-compensate modulator limited bandwidth or to pre-distort positions of different coding levels to compensate nonlinear DC-characteristic of the modulator. The half-rate input interface for data and clock is obtained with the integration of driving buffer with three multiplexing stages. Well-opened PAM-2 eyes have been measured for all bits at 100 GBd. It provides adjustable output voltage with the differential amplitude up to about 2/3.7/4 V_{pp_diff} for PAM-2/4/8 operation respectively. In Fig.3 differential electrical output eye measurements are presented in these three operation formats. This IC has been packaged in a compact module with GPPO connectors (8 at the input and two at the output) as shown in Fig. 2. Power supplies are provided by an external bias board. Packaged SPDAC was measured up to 100 GS/s.



a) 100 GBd PAM-2 b) 100 GBd PAM-4 c) 84 GBd PAM-4 d) 64 GBd PAM-8 e) 50 GBd PAM-8

Fig. 3 SPDAC electrical differential outputs (on-wafer measurements)

4. Optical system experiments enabled by Power-DAC modules

The first experiment using PDAC was presented at OFC 2011's post-deadline paper session. A single-carrier 21.4-GBd PDM 64-QAM signal (256.8-Gb/s line rate), achieving 400-km single-channel transmission, was reported

in [10]. This component was also used to quantify, through simulations and experiments, the effect of in-band crosstalk on several advanced optical modulation formats [11]. In the following years, the progress in performances of PDAC device together with improvement and evolution of optical system architectures allowed a series of important experiments. In [12] the first WDM transmission of 50-GHz-spaced single-carrier 400-Gb/s channels using 43-GBd PDM-64QAM, at 8-b/s/Hz spectral efficiency, was reported with twenty channels sent over 600 km. In [13] the new algorithm based on artificial neural network approach was validated in experiment where a 84-GBd PAM-4 signal was transmitted over 1.5 km of SSMF, showing up to 10-fold improvement of BER. PDAC-based drivers showed ability to be used with different types of modulators, formats and transmitting media. In [14], a low-cost EAM-based transmitter was driven at 56-GBd PAM-4 signal and successfully transmitted over 2 km. In [15], record serial transmission rate of 42.8 Gbit/s PAM-4 data over a low-loss electrical backplane with PDAC component was reported. Two experiments with highest symbol rate were presented in [16] and [17]. In 2015 [16], first all-ETDM single-carrier and single-modulator 1.08-Tb/s (90-GBd PDM-64-QAM) transmitter was demonstrated using SPDAC modules. After 2:1 multiplexing of 45-Gb/s signals, electrical 90-GBd PAM-8 4-V_{pp} differential output signals are driving an I/Q modulator. At the Rx side, the high-speed coherent intradyne receiver is connected to 160-GS/s real-time oscilloscopes for off-line DSP. In 2016 [17], a single-carrier, single-polarization, intensity modulation and direct-detection transceiver for intra-datacenter networks was reported. Half-rate (42 and 50-Gb/s) input signals are multiplexed and coded to produce 84-GBd and 100-GBd PAM-4 outputs. C-band transmission over 1 km and 500 m was demonstrated.

Conclusion and perspectives

We presented the Power DAC concept, realizations and main experiments enabled by this component. This circuit operates up to 100 GS/s and can provide high swing electrical driving output in PAM-2/4/8.

The first implementation of SPDAC architecture allowed a series of record-breaking experiments. In coming realization, we'll consolidate and enhance this architecture by implementing additional features in particular: higher speed 2:1 multiplexers, integration of improved equalization functionalities, enhanced compensation of nonlinear and non-symmetric modulator characteristics (especially EAMs).

This new implementation will further enhance the development of next generation Tb/s transmitters with high spectral efficiency for datacenter and long haul applications.

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